BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

As rescanning documents *will not* correct images, please do not report the images to the Image Problem Mailbox.

(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: 0 395 146 A1

(12) EUROPEAN PATENT APPLICATION

(21) Application number: 90200966.1

(51) Int. Cl.5: H03K 17/687

(22) Date of filing: 19.04.90

(30) Priority: 25.04.89 NL 8901033

(43) Date of publication of application:
31.10.90 Bulletin 90/44

(84) Designated Contracting States:
DE FR GB

(71) Applicant: N.V. Philips' Gloeilampenfabrieken
Groenewoudseweg 1
NL-5621 BA Eindhoven(NL)

(72) Inventor: Stekelenburg, Michael Alwin Michael
c/o INT. OCTROOIBUREAU B.V., Prof. Holstlaan 6
NL-5656 AA Eindhoven(NL)

(74) Representative: van Gils, Cornelis Johannes Maria et al
INTERNATIONAAL OCTROOIBUREAU B.V.
Prof. Holstlaan 6
NL-5656 AA Eindhoven(NL)

(54) Control circuit for at least one clock electrode of an integrated circuit.

(57) The control circuit has two semiconductor switches (PT, NT) which are controllable from a clock pulse generator (CG) via which switches one of two direct voltages (+Va, oV) is periodically applied to a clock electrode (E), constituting a capacitive load, of an integrated circuit (IC). To realise a reduced energy dissipation, the clock electrode (ET) is connected to ground via a series arrangement (LC) of an inductance (L) and a capacitance (C) and a clock pulse supply is effected at which the switches (PT, NT) are successively conducting with an interval thereinbetween in which both switches are non-conducting. As a result, a resonant circuit (L, C, CE) of the inductance (L), the capacitance (C) and the clock electrode capacitance (CE) is active during the intervals.

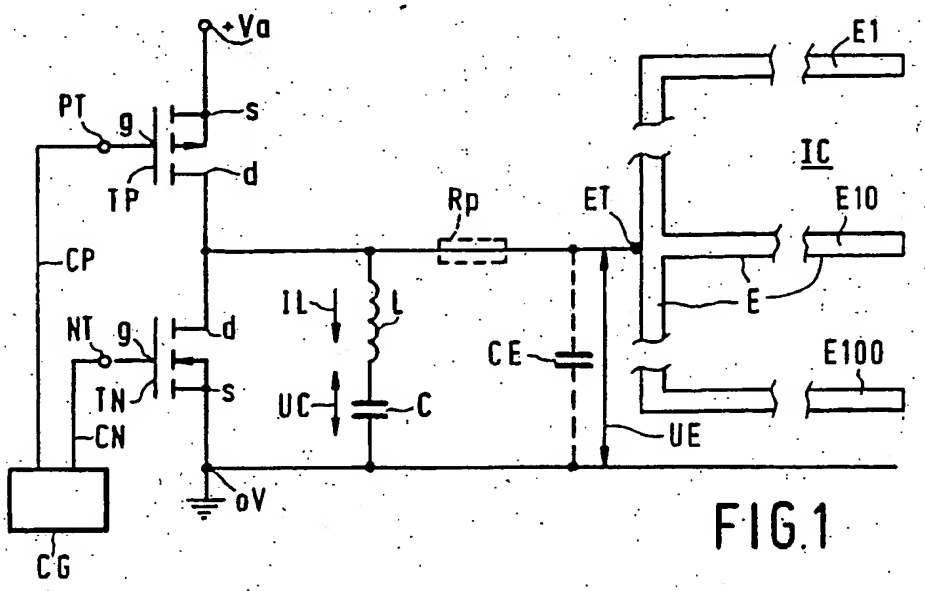

FIG.1

EP 0 395 146 A1

The invention relates to a control circuit for at least one clock electrode, constituting a capacitive load, of an integrated circuit, which control circuit comprises at least two controllable semiconductor switches each having an output coupled to a terminal of the clock electrode, an input coupled to an associated terminal for connection to an associated direct voltage and a control input coupled to an associated terminal for coupling to a clock pulse generator so that the clock electrode is periodically switchable between two direct voltages.

A control circuit of this type for an integrated circuit particularly implemented as an image sensor is known from an Article in Philips Technical Review, vol. 43, no. 1/2, December 1986, pp. 1 to 8, entitled "The accordion imager, a new solid-state image sensor". The two semiconductor switches are in the form of MOS transistors in which the output is a drain electrode, the input is a source electrode and the control input is a gate electrode. A first MOS transistor is of the p-channel type and a second is of the n-channel type and they are arranged in series between a terminal conveying a higher direct voltage and a terminal conveying a lower direct voltage. The gate electrodes are interconnected and are connected to the drain electrode of a third MOS transistor whose gate electrode is connected to the clock pulse generator. The three transistors jointly constitute an element of a shift register in which the gate electrode of the third transistor is connected to the drain electrodes of the first and second transistors of the previous shift register element. The described shift register implementation of the control circuit is specific of the so-called accordion control of the image sensor.

Apart from the specific implementation of the control circuit described it appears that the clock electrode is periodically switched between the higher direct voltage and the lower direct voltage. The clock electrode then has a capacitance which is periodically charged and discharged via a series resistor. The series resistor not only comprises the source drain resistor of the conducting transistor but also parasitic series resistors. Recharging of the clock electrode capacitance is thereby accompanied by dissipative losses. These losses are dependent on many factors, particularly on the height of the clock pulse frequency, the number of clock pulse phases, the values of the capacitances provided and the voltage difference between the higher and the lower voltage. The energy dissipation is not only unwanted because of its character of energy loss, but also because of heating of the integrated circuit.

It is an object of the invention inter alia to provide a control circuit for a clock electrode of an integrated circuit in which the energy dissipation is reduced. To this end a control circuit according to the invention is characterized in that a terminal of the clock electrode in the control circuit is coupled to a DC terminal via a series arrangement of an inductance and a capacitance, whereby this inductance, together with this capacitance and a clock electrode capacitance constitute a resonant circuit, said clock pulse generator being suitable for supplying clock pulses to the control inputs of the semiconductor switches so that these are periodically and successively conducting with an interval thereinbetween in which both switches are non-conducting.

Due to the measure according to the invention the energy in the clock electrode capacitance is stored temporarily in the inductance of the resonant circuit so that this energy can be used again, which may lead to a considerable reduction of energy consumption.

It is to be noted that an inverter circuit for an inductive load comprising a gas discharge lamp in series with a coil and a bridge capacitor is known per se from DE-A 38.13.672, with a capacitor being arranged parallel to this series arrangement. This capacitor serves to suppress interference upon neighbouring radio receivers. However, the L-C series arrangement according to the present invention serves to reduce the energy dissipation in the integrated circuit.

The invention will be described by way of example with reference to the accompanying drawing in which

Fig. 1 shows diagrammatically an embodiment of a control circuit according to the invention and

Fig. 2 shows some time diagrams of voltages and a current to explain the operation of the circuit of Fig. 1.

In Fig. 1 the reference IC denotes an integrated circuit only a clock electrode E of which is shown partly. The integrated circuit IC may be in the form of an image or line sensor, a delay line, a memory, etc., for example, operating as a charge transfer device. The references E1, E10 and E100 denote some clock electrode strips which are present on or in the circuit IC and which may form part of the electrode E. The electrode E may also be in the form of a single strip. The reference ET denotes a terminal of the electrode E and a clock electrode voltage is denoted by UE between this terminal and a ground connection (oV). With respect to ground conveying the ground potential of oV, the electrode E has a capacitance which is denoted by CE. The clock electrode capacitance CE is assumed to comprise parasitic capacitances. The clock electrode terminal ET is coupled to a junction point of two controllable semiconductor switches TP and TN shown as MOS transistors. The switch

to be further described as transistors TP and TN is of the p and of the n-channel type, respectively, as has been illustrated by means of an arrow head in a substrate connection of the transistor. Outputs of the transistors TP and TN shown as drain electrodes d are coupled to the clock electrode terminal ET. Inputs of the transistors TP and TN shown as source electrodes s are coupled to terminals conveying a direct voltage +V1 and oV, respectively. Control inputs of the transistors TP and TN shown as gate electrodes g are coupled to terminals PT and NT, respectively, of a clock pulse generator CG. The generator CG applies clock pulse signals CP and CN to the terminals PT and NT, respectively. Assuming that the clock pulse signals CP and CN in the control circuit described so far are two clock pulse signals occurring in phase opposition and having the same variation, this circuit is known. However, according to an aspect of the invention the clock pulse signals CP and CN are not in phase opposition, which is illustrated by means of the signal variation shown in Fig. 2. Fig. 2 shows time diagrams as a function of time t with instants t1 to t9. The clock pulse signals CP and CN show a voltage variation between +Va and oV. The voltage of oV is present between the instants t2 and t3, and t8 and t9 in the signal CP and during these periods the transistor TP is turned on between the terminal conveying the voltage +Va and the terminal ET, while due to CN = oV the transistor TN is turned off. The voltage of +Va is present between inter alia the instants t5 and t6 in the signal CN, the transistor TN being turned on while due to CP = +Va the transistor TP is turned off. Between the instants t3 and t5, and t6 and t8, with CP = +Va and CN = oV the two transistors TP and TN are turned off. The intervals between t3 and t5 and between t6 and t8 at the clock pulse signals CP and CN are an aspect of the invention.

According to another aspect of the invention the terminal ET of the clock electrode E is coupled to a DC terminal via a series arrangement (L, C) of an inductance L and a capacitance C. According to Fig. 1 this is the terminal conveying the ground potential of oV. The series arrangement (L, C) may alternatively be connected to a terminal conveying a different voltage. The reference IL denotes a current through the inductance L. The reference UC denotes a voltage across the capacitance C. The capacitance C may be present in the form of a capacitor in the control circuit or it may form part of the integrated circuit IC. The reference Rp denotes a parasitic resistance between the junction point of the transistors TP and TN and the inductance L and the clock electrode terminal ET. The resistance Rp is assumed to comprise all series resistors which exert influence when recharging the clock electrode capacitance CE. The inductance L and the capacitances C and CE jointly constitute a resonant circuit (L, C, CE) in which the parasitic resistance Rp occurs.

Fig. 2 shows the voltage variation of the voltages UE and UC and the current variation of the current IL. The current IL has a more or less cosine-shaped variation between the instants t2 and t8 with respect to a zero current oA. In this case the voltage UC has a small voltage variation. The value of the voltage variation is dependent on the value of the capacitance C with respect to the value of the clock electrode capacitance CE. If the capacitance C has a value which is a factor of the order of five larger than the value of the capacitance CE, the voltage UC can be considered to be substantially constant. The voltage UE has a signal variation at which the voltage +Va and the voltage oV are present via the conducting transistors TP (t2 to t3, and t8 to t9) and TN (t5 to t6), respectively. The resonant circuit (L, C, CE) is active during the intervals between the instants t3 and t5 as well as t6 and t8 with the transistors TP and TN being non-conducting. The references t1, t4 and t7 denote the intermediate instants of three intervals at which the current IL is maximum. Fig. 2 shows an overshoot caused by the resonant circuit (L, C, CE) at the instants t2, t5 and t8. The edge steepness of the overshoot is substantially determined by the value of the inductance L.

Fig. 2 shows that the time difference (t3 - t2) is smaller than the time difference (t6 - t5). Consequently, the time difference (t4 - t1) is smaller than the time difference (t7 - t4). The quotient of the time difference (t4 - t1) and the time difference (t7 -t1) which is equal to the clock pulse period of the signals CP and CN determines the duty cycle of the transistors TP and TN.

As compared with the known method of recharging the clock electrode capacitance C1, the use of the resonant circuit (L, C, CE) leads to a saving in energy.

The instants t2 and t5 at which the transistors TP and TN must be turned on under the control of the clock pulse signals CP and CN, respectively, are not critical due to the use of the MOS transistors TP and TN shown. This is due to the presence of a drain substrate diode in the MOS transistors. This diode becomes conducting before the instants t2 and t5 at the transistors TP and TN, respectively. This yields a further saving in energy because the source-drain voltage is decreased at the instant when the transistor is turned on. When using bipolar transistors instead of the MOS transistors TP and TN, a parallel diode may be arranged across the transistor so as to realise a non-critical turn-on.

Fig. 1 shows a single clock electrode terminal

ET for connection to the drain electrode d of the respective transistors TP and TN and the series arrangement (L, C). Instead, two or three terminals can be arranged proximate to or remote from each other at the integrated circuit IC.

If desired, parts of the control circuit can be integrated in the integrated circuit. The inductance L may be constituted in known manner by a gyrator circuit and a capacitance. In this case even the entire control circuit can be integrated in the integrated circuit.

Claims

1. A control circuit for at least one clock electrode, constituting a capacitive load, of an integrated circuit, which control circuit comprises at least two controllable semiconductor switches each having an output coupled to a terminal of the clock electrode, an input coupled to an associated terminal for connection to an associated direct voltage and a control input coupled to an associated terminal for coupling to a clock pulse generator so that the clock electrode is periodically switchable between two direct voltages, characterized in that a terminal of the clock electrode in the control circuit is coupled to a DC terminal via a series arrangement of an inductance and a capacitance, whereby this inductance, together with this capacitance and a clock electrode capacitance constitute a resonant circuit, said clock pulse generator being suitable for supplying clock pulses to the control inputs of the semiconductor switches so that these are periodically and successively conducting with an interval thereinbetween in which both switches are non-conducting.

2. A control circuit as claimed in Claim 1, characterized in that the said capacitance has a value which is a factor of the order of five larger than the value of the clock electrode capacitance.

fährt weg:
Es sollen sinus-
ähnliche Schwingungen
erzeugt werden!

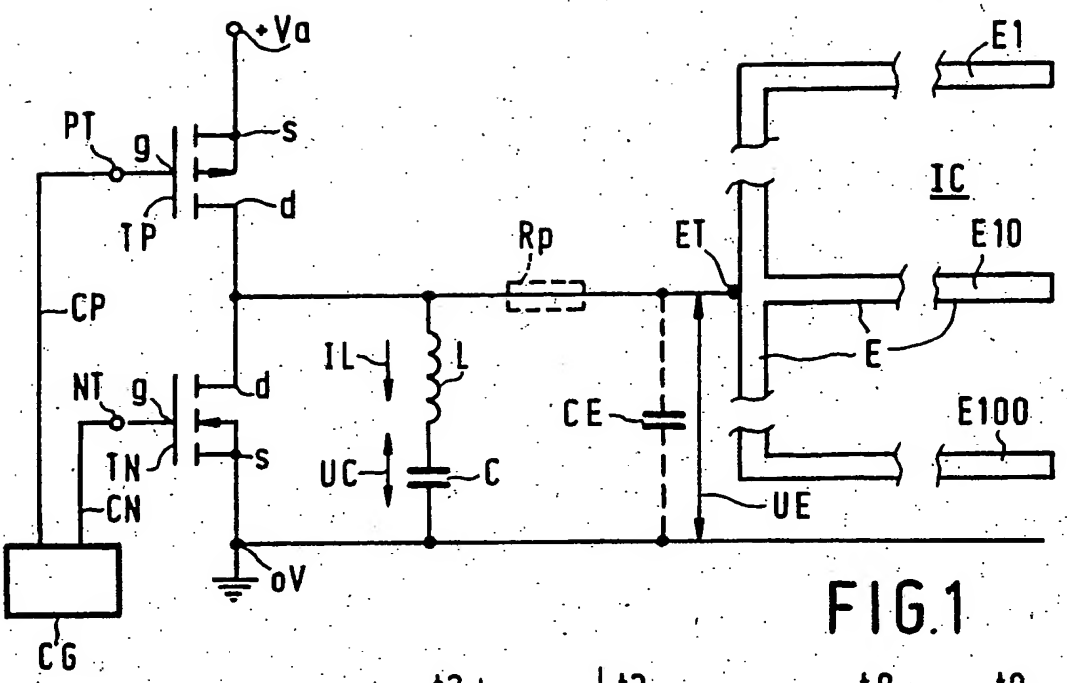

FIG.1

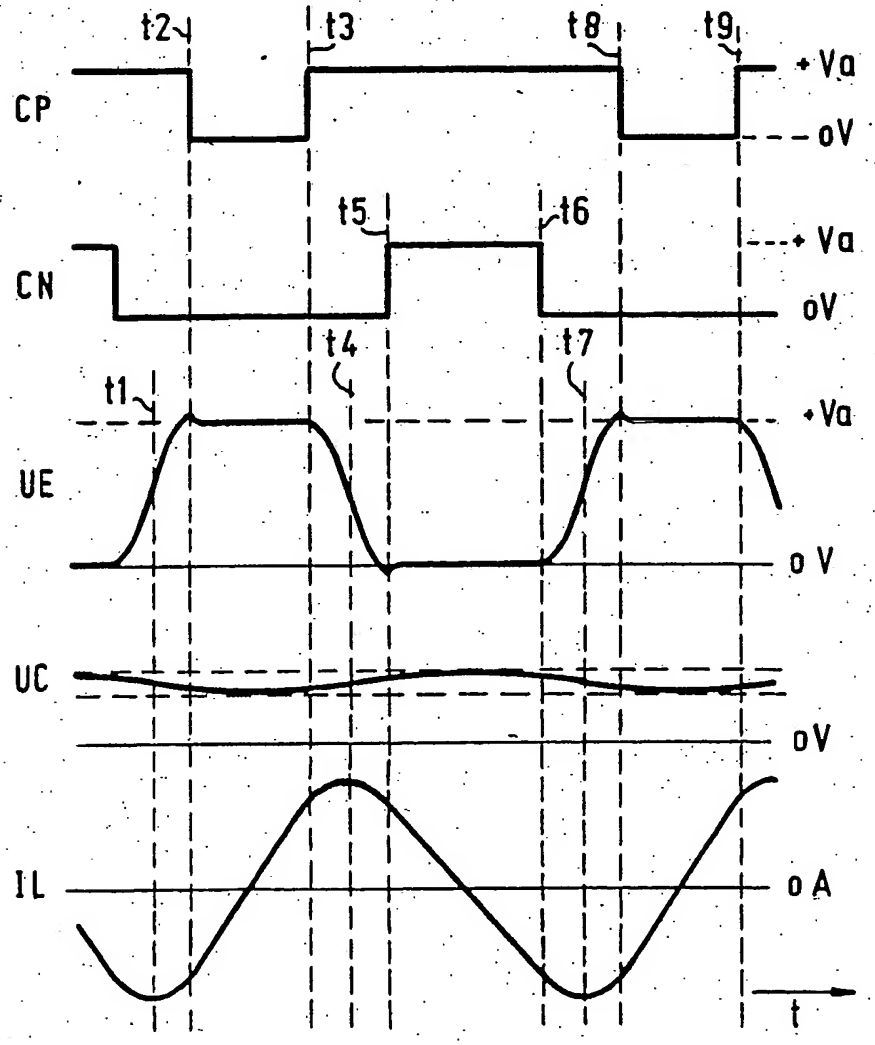

FIG.2

European Patent Office

EUROPEAN SEARCH REPORT

Application Number

EP 90 20 0966

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
X,D	DE-A-3 813 672 (SIEMENS AG) * Column 3, line 63 - column 4, lines 1,14-22; column 6, line 29 - column 9, line 38; figures 4,5 *	1	H 03 K 17/687

TECHNICAL FIELDS SEARCHED (Int. Cl.5)

H 03 K
H 03 F

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	24-07-1990	CANTARELLI R.J.H.

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P0401)